

INFORMATION DISCLOSURE STATEMENT (IDS)

For USPTO Patent Application — PT-NPU Architecture

Application Number: [To Be Assigned — File US Provisional First] **Filing Date:** [Filing Date] **Title:** PARALLEL TEMPORAL-LOGIC NEUROMORPHIC PROCESSING UNIT (PT-NPU) WITH PREDICTIVE SPIKING NEURAL NETWORK ARCHITECTURE
Inventor: Chaipayop Ninphet (The Architect) **Applicant:** [Applicant Name]

Instructions for Filing

1. Use **PTO/SB/08** (or **PTO/AIA/08** for AIA applications) form
 2. Submit this IDS within **3 months** of filing date
 3. If filing US Provisional, IDS may be submitted later with non-provisional
 4. Each reference listed must be **actually considered** by the Examiner
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SECTION A — U.S. PATENTS (สิทธิบัตรสหรัฐฯ ที่ เกี่ยวข้อง)

No.	Patent Number	Date	Inventor/Assignee	Title
1	US 10,489,672 B2	2019-11-26	Intel Corp.	Asynchronous Neuromorphic Processor

No.	Patent Number	Date	Inventor/Assignee	Title
2	US 9,558,428 B2	2017-01-31	IBM Corp.	Neural Core Circuit
3	US 10,762,419 B2	2020-09-01	IBM Corp.	Digital STDP Synapse and LIF Neuron-based Neuromorphic System
4	US 11,151,441 B2	2021-10-19	Knowm Inc.	System and Method for Spontaneous Machine Learning
5	US 2020/0401876 A1	2020-12-24	HRL Laboratories	Scalable Energy-Efficient Analog Neuromorphic Processors
6	US 2025/0278621 A1	2025-09-04	Samsung Electronics	Neuromorphic Computing Device
7	US 2025/0348727 A1	2025-11-13	[Assignee]	Unsupervised Learning of Memristor Crossbar Neuromorphic
8	US 2025/0169081 A1	2025-05-22	[Assignee]	Memristive Structure, Memristive Array
9	US 2025/0149087 A1	2025-05-08	[Assignee]	Crossbar Array with Reduced Disturbance
10	US 2024/0417621 A1	2024-05-16	IBM Corp.	Compensating Non-ideality of

No.	Patent Number	Date	Inventor/Assignee	Title
				Neuromorphic Memory Device

SECTION B — U.S. PATENT APPLICATION PUBLICATIONS

No.	Publication No.	Date	Inventor/Assignee	Title
11	US 2019/0147552 A1	2019-05-16	[Assignee]	Neuromorphic Processor with Memristive Crossbar Array
12	US 2025/0284939 A1	2025-09-11	[Assignee]	Spiking Neural Networks
13	US 2025/0292072 A1	2025-09-18	Samsung Electronics	Neuromorphic Computing Device Using SNN
14	US 2013/0297542 A1	2013-11-07	Brain Corp.	Sensory Input Processing in SNN
15	US 2025/0272550 A1	2025-08-28	[Assignee]	Memristive Self-Learning STDP Neural Networks

SECTION C — FOREIGN PATENTS (สิทธิบัตรต่างประเทศ)

No.	Patent Number	Country	Date	Title	Relevance
16	EP 3 293 681 A1	European	2018-03-14	Spatio-temporal SNN in Neuromorphic Hardware	Temporal sy circuits; STD ไม่ใช่ deriva
17	WO 2024/153705 A1	PCT	2024-07-25	Self-timed Feedforward Mixed-Signal Neurons	Self-timed L derivative/
18	WO 2025/017094 A1	PCT	2025-01-23	Method to Build and Deploy SNN on Hardware	Hardware-a' deployment not device
19	WO 2020/099583 A1	PCT	2020-05-22	Spiking Neural Network	SNN learnin software ap
20	KR 10-2024-0029909	Korea	2024-02-29	Neuromorphic Computing Device (priority doc)	Memristor convolution US 2025/02

SECTION D — NON-PATENT LITERATURE (บทความวิชาการ)

No.	Reference	Date	Relevance
21	Q. Xia and J. J. Yang, "Memristive Crossbar Arrays for Brain-Inspired Computing," <i>Nature</i>	2019-04	Foundational review of memristor crossbar; แต่ไม่มี การซ้อน 3D หรือ monolithic BEOL

No.	Reference	Date	Relevance
	<i>Materials</i> , Vol. 18, pp. 309-323, 2019.		
22	M. Davies et al., "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," <i>IEEE Micro</i> , Vol. 38, No. 1, pp. 82-99, 2018.	2018-01	Intel Loihi Architecture; AER + SNN แต่ใช้ SRAM + LIF
23	P. A. Merolla et al., "A Million Spiking-Neuron Integrated Circuit with a Scalable Communication Network and Interface," <i>Science</i> , Vol. 345, No. 6197, pp. 668-673, 2014.	2014-08	IBM TrueNorth; 1M neurons, LIF , ไม่มี prediction
24	G. Indiveri et al., "Neuromorphic Silicon Neuron Circuits," <i>Frontiers in Neuroscience</i> , Vol. 5, Art. 73, 2011.	2011-05	Survey of analog neuron circuits; รวม LIF/I&F/Adaptive , ไม่มี PIF
25	C. Li et al., "Analogue Signal and Image Processing with Large Memristor	2018-01	Analog MVM with memristor crossbar; ระบบ 2D , ใช้ software processing

No.	Reference	Date	Relevance
	Crossbars," <i>Nature Electronics</i> , Vol. 1, pp. 52-59, 2018.		
26	S. B. Eryilmaz et al., "Brain-like Associative Learning Using a Nanoscale Non-Volatile Phase Change Synaptic Device Array," <i>Frontiers in Neuroscience</i> , Vol. 8, Art. 205, 2014.	2014-07	Phase-change memristive synapse; ไม่มี integration กับ CMOS neuron
27	J. Pei et al., "Towards Artificial General Intelligence with Hybrid Tianjic Chip Architecture," <i>Nature</i> , Vol. 572, pp. 106-111, 2019.	2019-08	Hybrid neuromorphic/AI chip; architectural, ไม่มี PIF
28	W. Maass, "Networks of Spiking Neurons: The Third Generation of Neural Network Models," <i>Neural Networks</i> , Vol. 10, No. 9, pp 1659-1671, 1997.	1997-12	Foundational paper; LIF/Izhikevich models, ไม่มี predictive firing

No.	Reference	Date	Relevance
29	E. M. Izhikevich, "Simple Model of Spiking Neurons," <i>IEEE Trans. Neural Networks</i> , Vol. 14, No. 6, pp. 1569-1572, 2003.	2003-11	Izhikevich neuron model; ยังเป็น software/差分方程, ไม่ใช่ hardware circuit
30	A. Shaban et al., "Trimming the Fat: A Fine-Tuning Approach to Leaky Integrate-and-Fire Neurons for Efficient Spiking Neural Networks," <i>Frontiers in Neuroscience</i> , 2022.	2022	LIF optimization; เป็น software training technique

SECTION E — REFERENCES CITED IN PRIOR ART SEARCH REPORT

No.	Reference	Source	Date
31	US 2025/0348727 A1 — "Unsupervised Learning of Memristor Crossbar Neuromorphic Processing Systems"	USPTO Patents-Review	2025-11-13
32	US 2025/0278621	USPTO Patents-	2025-09-04

No.	Reference	Source	Date
	A1 — "Neuromorphic Computing Device" (Samsung)	Review	
33	US 2024/0417621 A1 — "Compensating Non-ideality of a Neuromorphic Memory Device"	USPTO	2024-12-19
34	US 2025/0149087 A1 — "Crossbar Array with Reduced Disturbance"	USPTO	2025-05-08
35	US 2025/0169081 A1 — "Memristive Structure, Memristive Array"	USPTO	2025-05-22
36	US 2025/0272550 A1 — "Memristive Self-Learning Spiking Feedback Loops-Based Neural Networks with STDP"	USPTO	2025-08-28

SUMMARY OF DISTINCTIONS (สาระสำคัญที่แยกจากการประดิษฐ์นี้)

What distinguishes the present invention from all cited prior art:

Aspect	Prior Art	Present Invention (PT-NPU)
Neuron Firing	Reactive (LIF/IF): fires when V_{mem} reaches threshold	Predictive (PIF): fires when $V_{\text{pred}} = V_{\text{mem}} + \alpha \cdot dV/dt + \beta \cdot d^2V/dt^2 \geq \text{threshold}$
Derivative Computation	None (membrane dynamics only)	Hardware first + second derivative circuits (active RC differentiators)
Synapse Implementation	SRAM, PCM, or 2D memristor crossbar	3D monolithic BEOL memristor crossbar, 4-16 layers stacked
Memory Access	SRAM/DRAM off-chip or on-chip (partial Von Neumann)	Zero off-chip memory access (true in-memory computing)
Communication	Clocked or partially synchronous	Fully asynchronous AER + fine-grained power gating (~0W idle)
Security	None or general IC security only	Neuromorphic-specific: decoy spikes + PUF routing + power noise + anti-tamper
Firing Mode	Single mode (reactive)	Dual mode: predictive + reactive (fallback)
Integration	Separate die or 2.5D	Monolithic 3D: CMOS + BEOL memristor + micro-cooling on single die

CERTIFICATION (คำรับรอง)

I hereby certify that each of the references listed above was cited in an Information Disclosure Statement filed with the USPTO on the dates indicated. I also certify that I am aware of the duty to disclose information material to patentability as defined in 37 CFR § 1.56.

Signature: _____ **Name:** Chaiyapop
Ninphet **Date:** _____

ATTACHMENT: Filing Form PTO/SB/08

Note: Transfer these references to PDF form PTO/SB/08 (or EFS-Web IDS) for official submission.

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Disclaimer: This IDS is prepared based on patent search conducted on [Date]. Additional prior art may exist. The duty of candor under 37 CFR § 1.56 requires disclosure of all material prior art known to the inventor. This list is not guaranteed to be exhaustive.